

Appl. No. 10/761,564
Amdt. dated February 1, 2007
Reply to Office Action of November 2, 2006

Amendments to the Drawings:

Included in the amendment are an "Annotated Sheet Showing Changes" and a "Replacement Sheet" for Figs. 2 and 3.

In Fig. 2, the S/P-bit has been changed to SP/PE-bit as suggested by the Examiner.

In Fig. 3, the column label S/P in table 310 and the column label S/P in the control specification 300 have been changed to SP/PE as suggested by the Examiner.

Appl. No. 10/761,564
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Remarks

The present amendment responds to the final Official Action dated November 2, 2006. The Official Action objected to the specification, drawings, and claims due to informalities and inconsistencies. Claims 14, and 16-29 were rejected under 35 U.S.C. § 112. The objections and the grounds of rejection are addressed below.

Claims 14, 16, 19, 24, 26, and 27 have been amended to be more clear and distinct. Claims 14 and 16-29 are presently pending.

Changes to the Specification

The paragraphs beginning at page 3, line 2, page 3, line 11, page 3, line 20, page 4, line 16, page 4, line 18, page 9, line 18, page 10, line 11, page 11, line 6, and page 18, line 3 were amended to replace all occurrences of S/P with SP/PE as suggested by the Examiner.

The paragraph beginning at page 9, line 18 has also been amended to correct a typographical error, changing "SP configurable register file 214" and "PE configurable register file 216" to SP reconfigurable compute register file 214 and PE reconfigurable compute register file, respectively, for consistency with Fig. 2.

Objections to the Claims

In claims 14 and 19 the "context status bit" and in claim 24, the "context select bit" have been changed to "context switch bit" to be consistent with the specification. See, page 4, lines 16-17 and page 9, line 20 of the specification.

Appl. No. 10/761,564
Amdt. dated February 1, 2007
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Claim 14 has been amended changing "a control processor" to "a sequence processor (SP)" to be clear that the "SP and at least one PE combined to form a combined processor" as claimed. Support for this change for consistency and clarity can be found in Fig. 1 that contains a "controller sequence processor (SP) combined with processing element-0 (PE0) SP/PE0 101". See also page 7, lines 15-17, for example.

In claims 14 and 19, "the SP having a set of control register files" has been changed to "the SP having a set of SP register files" to conform to the specification and figures. For example, see, Figs. 1, 2, and 5 and page 8, lines 19-20, page 10, lines 1-2, and page 12, lines 11-15.

Claim 14 has also been amended as suggested by the Examiner changing "stored on the set" to "stored in the set" in the third and fourth paragraphs of the claim.

Claim 16 has been amended changing "the set of control register files" to "the set of SP register files" to conform with the amended claim 14.

Claim 19 has been amended to correct a grammatically incorrect phrase by removing "wherein" from the phrase "wherein the combined processor having substantially similar access..." as suggested by the Examiner. Claim 19 has also been amended as suggested by the Examiner changing "stored on the set" to "stored in the set" in the last two paragraphs of the claim.

Claim 24 has been amended changing "an PE" to "a PE" in the last paragraph of the claim as suggested by the Examiner.

Appl. No. 10/761,564
Amdt. dated February 1, 2007
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Claim 26 has been amended as suggested by the Examiner changing "a SP" to "an SP" in line 2 of the claim.

Claim 27 has been amended as suggested by the Examiner changing the phrase "a PE machine state register files" to "a PE machine state register file".

Section 112 Rejection

Claims 14 and 19 were rejected as being unclear regarding the phrase "substantially similar access" as used in the claims "the combined processor having substantially similar access to the set of SP register files and to the set of PE register files of the at least one PE that was combined to form the combined processor". The phrase "substantially similar access" refers, for example, to Fig. 2 and selectably writing data "either to the SP reconfigurable compute register file 214 or to the PE reconfigurable compute register file 216" and to selectably reading data from "registers 214 or 216". The selectable writing of data is enabled through "enable signals 204 and 206 to multiplexers 208 and 210, respectively" to control which register file to write to. The selectable reading of data is enabled through "a select signal 218 to a multiplexer 220 to control which block of registers 214 or 216" to "read data from". See Fig. 2 and page 9, line 22 to page 10, line 4. It is further noted that "both of the reconfigurable register files" of Fig. 2 are in reference to the "controller sequence processor (SP) combined with processing element-0 (PE0) SP/PE0 101" combined processor that is "shown in Fig. 1". See Figs. 1 and 2, and page 7, line 17 and page 10, lines 6-10.

Appl. No. 10/761,564
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While equivalent access may be provided to both the SP register files and the PE register files through the multiplexers 208, 210, and 220, the access to the register files further depends upon the "separate selection and control" enable signals 204 and 206 and select signal 218 which depend "upon the instruction in execution and the machine state" which may vary from program to program. Thus, the term "substantially similar access" was used. See, page 10, lines 6-10.

While it is believed the present language is clear in context, alternative language can be considered if the Examiner feels it will be clearer. In the later case, please call the undersigned.

Claim 19 has also been amended to clear up an antecedent basis problem as indicated by the Examiner, changing "the set of compute register files" to "the set of PE register files".

Claim 24 has been amended to correct the antecedent basis for "the instruction" in line 15 to "each instruction". Claim 24 has been further amended to make clear that "an SP instruction" is "one of the at least two instructions" and that "a PE instruction" is "the other instruction of the at least two instructions".

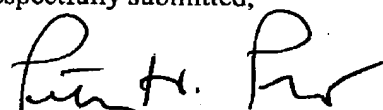
Since dependent claims 16-18, 20-23, and 25-29 depend from and contain all the limitations of the corresponding base claims, claims 14 and 16-29 are placed in order for allowance.

Appl. No. 10/761,564
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Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,

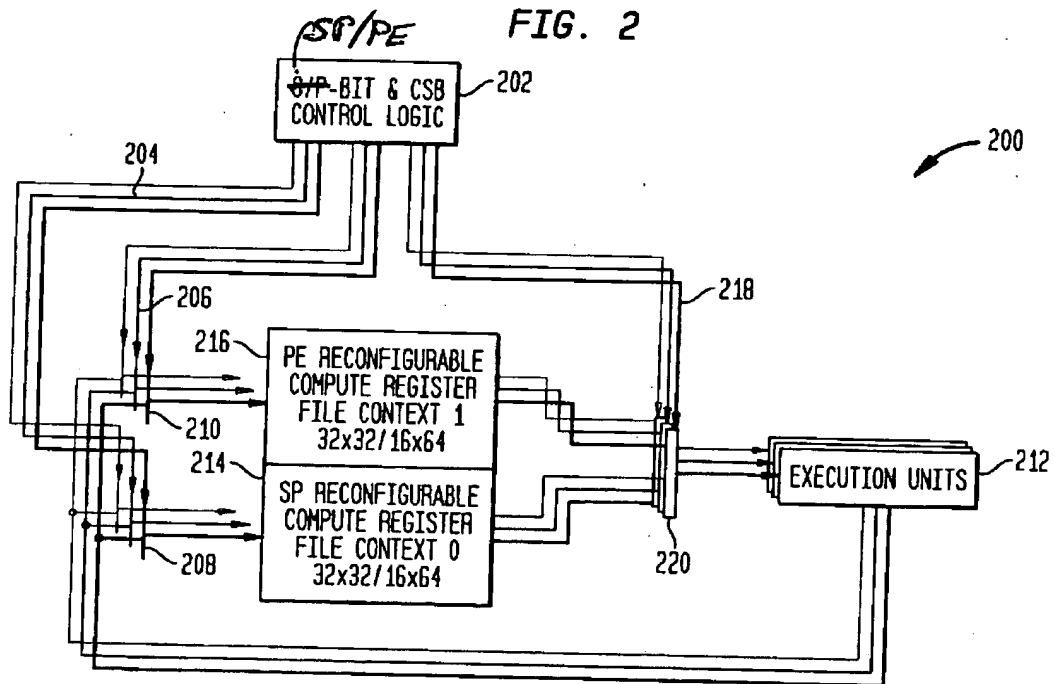


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SERIAL NO.: 10/761,564
PETER H. PRIEST (919-806-1600)

*Annotated Sheet
Showing Changes*

2/6



SERIAL NO.: 101761,564 *Annotated Sheet*
 PETER H. PRIEST (919-806-1600) *Showing Changes*

3/6

FIG. 3

SP/PE

MANARRAY ARCHITECTURE INSTRUCTION TYPE		OPERATING MxN		COMMENTS
SP	PE	CSB	SP/PE	
0	SP ONLY INSTRUCTION	0	0	SP INSTRUCTIONS USE ONLY THE SP'S CONTEXT-0 REGISTER FILES
1	PE ONLY INSTRUCTION	0	1	PE INSTRUCTIONS USE ONLY THE PE0'S REGISTER FILES
1	PE ONLY INSTRUCTION	1	0	SP INSTRUCTIONS USE ONLY THE PE0'S CONTEXT-1 REGISTER FILES
1	PE ONLY INSTRUCTION	1	1	PE INSTRUCTIONS TYPICALLY NOT USED
1	PE ONLY INSTRUCTION	0	0	SP INSTRUCTIONS USE ONLY THE SP'S CONTEXT-0 REGISTER FILES
1	PE ONLY INSTRUCTION	0	1	PE INSTRUCTIONS USE ONLY THE PE0'S AND PE1'S REGISTER FILES
1	PE ONLY INSTRUCTION	1	0	SP INSTRUCTIONS USE ONLY THE PE0'S CONTEXT-1 REGISTER FILES
1	PE ONLY INSTRUCTION	1	1	PE INSTRUCTIONS USE ONLY THE PE1'S REGISTER FILES
1	PE ONLY INSTRUCTION	0	0	SP INSTRUCTIONS USE ONLY THE SP'S CONTEXT-0 REGISTER FILES
1	PE ONLY INSTRUCTION	0	1	PE INSTRUCTIONS USE ONLY THE PE0-4'S REGISTER FILES
1	PE ONLY INSTRUCTION	1	0	SP INSTRUCTIONS USE ONLY THE PE0'S CONTEXT-1 REGISTER FILES
1	PE ONLY INSTRUCTION	1	1	PE INSTRUCTIONS USE ONLY THE PE1-4'S REGISTER FILES